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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/490,263	01/24/2000	Jing Wang		6937

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EXAMINER	
HUYNH, KIM T	
ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 07/02/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/490,263	Applicant(s) WANG ET AL.	
	Examiner Kim Huynh	Art Unit 2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-48* is/are rejected.

7)☒ Claim(s) *10 and 46* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Title

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

Claim 10 and 46 are objected to because of the following informalities: the term "USBD" is unclear; applicant is reminded to define the term "USBD".

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 4 recites the limitation "the Main processor". There is insufficient antecedent basis for this limitation in the claim.

Claim 7 and 8 recite the limitation "the USB bus". There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Madden et al. (U.S Patent 6,393,493)

Madden substantially discloses a USB host system (fig.3, 206) comprising:

- a first processor implementing a function of a USB driver. (fig.4, 226), (fig. 2, 180), (col. 5, lines 35-41)
- a downstream USB port. (col. 5, lines 35-41)
- a communication area accessible both by a second processor and by the first processor. (col.5, lines 8-13)
- where the communication area is a dual port memory. (fig.2, 144)
- where the communication area consists of multiple FIFO registers. (fig.7, 456)
- where an interrupt polled from a USB interrupt pipe is converted to an interrupt signal to the Main Processor. (col.3, lines 21-30)
- where the said second processor interfaces the host system via a standard microprocessor bus. (fig.2, 154), (col.3, lines 21-30)
- where a hub is used to provide multiple downstream USB ports. (col.5, lines 35-41)
- where data in the communication area are directly sent out on the USB bus. (col.6, lines 6-8)
- where data received from the USB bus (fig.1, 104) are written directly in the communication area. (col.4, lines 45-54)
- where the said host system is used to provide a USB host function to the said second processor. (fig.2, 154), (col.5, lines 31-37)
- where the said host system is used to provide a USB host function to the said second processor which runs an operating system supporting USB, by intercepting calls to the USBD in the said operating system. (col.6, lines 36-55, also see abstract)

- a first processor implementing a function managing a USB host controller. (fig.3, 206)

- an interface that provides a high-level USB pipe view of a USB system to a program running on a second processor; and (fig.4, 226), (col.6, lines 26-55)

- Where the said interface uses a memory that can be accessed by both the first processor and the second processor. (col.4, lines 45-54 and 65-67)

Claim 17-48 are rejected under 35 U.S.C. 102(e) as being anticipated by Pleso (U.S Patent 6,009,480)

Pleso substantially discloses an information processing system comprising:

- A first processor. (fig.1, 120)

- A data transfer host system comprising a second processor (fig.1, 20) implementing a first data transfer driver managing a data transfer between the said first processor and a device; a data transfer port for connecting a device to the said data transfer host system; and an interface (fig.1, 32) with the first processor that provides a high-level view of the data transfer process to the first processor. (col.4, lines 28-33 and 66-67), (col.7, lines 59-60)

- Where the said interface uses a memory area that can be accessed by both the said first processor and the said second processor. (fig.1, 20), (col.4, lines 66-67)

- where the said interface uses a memory area that can be accessed by both the said first processor and the said second processor. (fig.1, 20), (col.4, lines 66-67)

- where the said second processor is used to reduce the number of interrupts to the said first processor. (fig.1, 32), (col.4, lines 16-17)

- where the said second processor is used to reduce the frequency of interrupts to said first processor. (fig.1, 32), (col.5, lines 16-18), (col.10, lines 44-46)

- where the said first processor interfaces the data transfer host system via a standard microprocessor bus. (fig.1, 40), (col.4, lines 66-67)

- where a hub is used to provide multiple ports for connecting a plural of devices. (col.12, lines 37-40)

- where the said .first processor contains a second data transfer driver capable of managing the same said data transfer and a data transfer request by the said first processor to the said second data transfer driver is carried out by the said data transfer host system. (col.11, lines 19-35)

- a downstream USB port. (col.12, lines 18-31)

- a memory accessible by both the said first processor and an second processor external to the said USB host, whereby a first area of the memory with a first predetermined format is used for a first type of transfer, and a second area of the memory with a second predetermined format is used for a second type of transfer. (col.3, lines 6-32)

- a hub is connected to the downstream USB port so that multiple devices can be connected to the system. (col.12, lines 18-67)

- where a third area of the memory with a third predetermined format is used for reporting device connection, enumeration and removal to the second processor. (fig.5a and 5b), col.9, lines10-51)

- where the said third area is in a part of the said memory which is read-only to the second processor. (fig.3, 72 and 74), (col.6, lines 44-45), (col.8, lines 25-29)

- where a fourth area of the memory with a fourth predetermined format is used for sending a USB command to the said USB host. (col.8, lines 62-67), (col.11, lines 16-35)

- where the starting address of each memory area for a transfer is used to identify the transfer. (col. 10, lines 15-29), (col.11, lines 16-35), (col.12, lines 65-67)

- where the second processor allocates the size of a memory area for a transfer to fit the need of the transfer. (col.11, lines 16-27)

- where the second processor allocates the number of the said areas to fit the need of a transfer. (col.10, lines 15-50 and see figure 10)

- where the starting address of the said first area can be in different part of the memory. (col.15, lines 1-3) (col.10, lines 15-50 and see figure 10)

- where the starting address of the said second area can be in different part of the memory. (col.10, lines 15-50 and see figure 10)

- where the starting address of the said first and second area are in the same location of the memory. (col.10, lines 15-50 and see figure 10)

- where the said predetermined formats of the said first and second areas are the same. (col.10, lines 15-50 and see figure 10)

- where the starting address of the said first and second areas are stored at fixed locations of the memory. (col.10, lines 15-50 and), (col.15, lines 1-60)

- where the said second processor writes a transfer request in a said area in the memory and notifies the first processor with an interrupt signal. (col.8, lines 26-29), (col.8, lines 49-51)

- where the first processor writes the status or data of a transfer into a said area in the memory and notifies the said second processor with an interrupt signal. (fig.1, 32), (col.5, lines 16-17)

- where a single format of the said second area implements isochronous, interrupt and bulk transfers; and (col.11, lines 59-65), (col.8, lines 10-23)

- a memory accessible by both the said first processor and a second processor external to the said USB host, whereby the said second processor initiates a USB transfer by writing a transfer request, and data for the said transfer, if there is any, into a first area in the said memory,and the said first processor carries out the transfer, and writes the status of the said transfer, and data from the said transfer, if there is any, into a second area in the said memory. (col.3, lines 6-32), (col.10, lines 15-30), (col.11, lines 15-36)

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kim Huynh whose telephone number is (703)305-5384. The examiner can normally be reached on M-F 9am-7pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Peter Wong can be reached on (703)305-3477. The fax phone numbers for the organization where this application or proceeding is assigned are (703)746-7239 for regular communications and (703)746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)306-5631.

Kim Huynh

June 25, 2002

PETER WONG
SUPERVISORY PATENT EXAMINER
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